What is claimed is:

1. A high-speed image pickup method of a charge coupled device (CCD) type solid-state image pickup device including m horizontal lines with a plurality of pixels, a vertical transmission register, and a horizontal transmission register, where m is an integer greater than zero, the high-speed image pickup method comprising the steps of:

(a) applying a vertical transmission signal to the vertical transmission register in the form of a field transmission signal, thereby simultaneously transmitting charges accumulated at the plurality of pixels to the vertical transmission register;

(b) applying the vertical transmission signal to the vertical transmission register in the form of a line transmission signal, thereby transmitting a charge signal corresponding to each horizontal line in the vertical transmission register to the horizontal transmission register at a high speed, and applying a horizontal transmission signal to the horizontal transmission register, thereby outputting the charge signal of the horizontal transmission register;

(c) transmitting the charge signal of the vertical transmission register to the horizontal transmission register at a normal speed when a horizontal line of which the charge signal is transmitted is a first horizontal line, and applying the horizontal transmission signal to the horizontal transmission register, thereby outputting the charge signal of the horizontal transmission register; and

(d) transmitting the charge signal of the vertical transmission register to the horizontal transmission register at the high speed when a horizontal line of which the charge signal is transmitted is a second horizontal line, and applying the horizontal transmission signal to the horizontal transmission register, thereby outputting the charge signal of the horizontal transmission register.

2. The high-speed image pickup method of claim 1, wherein the first horizontal line is a horizontal line in an upper portion of an image of the CCD type solid-state image pickup device.

3. The high-speed image pickup method of claim 1, wherein the second horizontal line is expressed by a value obtained by subtracting the value of the first

horizontal line from m and indicates a horizontal line in a lower portion of the image of the CCD type solid-state image pickup device.

4. A high-speed image pickup controller of a charge coupled device (CCD) type solid-state image pickup device including m horizontal lines with a plurality of pixels, a vertical transmission register controlled by a vertical transmission signal, and a horizontal transmission register controlled by a horizontal transmission signal, where m is an integer greater than zero, the high-speed image pickup controller comprising:

a horizontal position generator for generating a vertical counter value indicating the position of a horizontal line in response to the vertical transmission signal, outputting a first horizontal signal when the vertical counter value is smaller than a threshold value n, where n is an integer greater than zero and $n < m$, indicating a first horizontal line, and outputting a second horizontal signal when the vertical counter value exceeds a threshold value m-n indicating a second horizontal line;

ORing means receiving the first and second horizontal signals and performing an OR operation on them to generate a selection signal;

an operation mode selector for receiving a system clock signal, counting the pulses of the system clock signal to generate a horizontal counter value, generating a first comparison signal when the horizontal counter value is the same as the value of a normal horizontal clock signal, which indicates the number of clock pulses of a single horizontal line during a normal operation, and generating a second comparison signal when the horizontal counter value is the same as the value of a high-speed horizontal clock signal, which indicates the number of clock pulses of a single horizontal line during a high-speed operation, the operation mode selector being controlled by a horizontal reset signal;

a multiplexer for selecting and outputting the second comparison signal as the horizontal reset signal when the selection signal has a first logical level and selecting and outputting the first comparison signal as the horizontal reset signal when the selection signal has a second logical level; and

a comparator for outputting the first logical level as the vertical transmission signal when the value of a vertical clock signal, which indicates the number of clock

pulses in the active interval of the vertical transmission signal, is smaller than the horizontal counter value, and outputting the second logical level as the vertical transmission signal when the value of the vertical clock signal exceeds the horizontal counter value.

5. The high-speed image pickup controller of claim 4, wherein the horizontal position generator comprises:

a vertical counter for generating the vertical counter value in response to the vertical transmission signal received from the comparator, the vertical counter being controlled by a vertical reset signal;

a first horizontal comparator for outputting the first horizontal signal when the vertical counter value is smaller than the threshold value n indicating the first horizontal line;

a second horizontal comparator for outputting the second horizontal signal when the vertical counter value exceeds the threshold value m-n indicating the second horizontal line; and

a vertical comparator for generating the vertical reset signal for resetting the vertical counter when the vertical counter value is the same as the value of a field line signal which indicates the number of horizontal lines of a single field.

6. The high-speed image pickup controller of claim 4, wherein the operation mode selector comprises:

a horizontal counter for receiving the system clock signal and generating the horizontal counter value under the control of the horizontal reset signal;

a first comparator for generating the first comparison signal when the horizontal counter value is the same as the value of the normal horizontal clock signal; and

a second comparator for generating the second comparison signal when the horizontal counter value is the same as the value of the high-speed horizontal clock signal.

7. The high-speed image pickup controller of claim 4, wherein the number of clock pulses of each of the vertical clock signal, the normal horizontal clock signal and the high-speed horizontal clock signal is predetermined by a user.

8. The high-speed image pickup controller of claim 4, wherein the first horizontal line is a horizontal line in an upper portion of an image of the CCD type solid-state image pickup device.

9. The high-speed image pickup controller of claim 4, wherein the second horizontal line is expressed by a value obtained by subtracting the value of the first horizontal line from m and indicates a horizontal line in a lower portion of the image of the CCD type solid-state image pickup device.

10. The high-speed image pickup controller of claim 4, wherein the active interval of the vertical transmission signal is an interval for which a charge signal of the vertical transmission register is transmitted to the horizontal transmission register.

11. A high-speed image pickup method of a complementary metal-oxide-silicon (CMOS) image sensor including m horizontal lines with a plurality of pixels and an analog-to-digital converter, where m is an integer greater than zero, the method comprising the steps of:

(a) applying a vertical selection signal in response to a vertical shift clock signal, thereby enabling a first horizontal line among the m horizontal lines;

(b) applying a vertical transmission signal, thereby outputting a charge signal of the first horizontal line to the analog-to-digital converter;

(c) applying a vertical erasure signal, thereby erasing the charge signal of the first horizontal line;

(d) shifting the vertical selection signal in response to the vertical shift clock signal, thereby enabling a second horizontal line;

(e) applying the vertical erasure signal, thereby erasing a charge signal of the second horizontal line;

(f) shifting the vertical selection signal in response to the vertical shift clock signal, thereby enabling a horizontal line following the first horizontal line; and

(g) applying the vertical transmission signal, thereby outputting a charge signal of the horizontal line following the first horizontal line to the analog-to-digital converter.

12. The high-speed image pickup method of claim 11, wherein the first horizontal line is an arbitrary horizontal line among the m horizontal lines.

13. The high-speed image pickup method of claim 11, wherein the second horizontal line is an arbitrary horizontal line between the first horizontal line and the m-th horizontal line.

14. The high-speed image pickup method of claim 11, wherein the vertical erasure signal is enabled twice during a single period of a horizontal synchronizing signal.

15. The high-speed image pickup method of claim 11, wherein a rate at which the vertical shift clock signal is enabled can be adjusted.

16. A high-speed image pickup controller of a complementary metal-oxide-silicon (CMOS) image sensor including m horizontal lines with a plurality of pixels and an analog-to-digital converter, where m is an integer greater than zero, the controller comprising:

a vertical shifter for receiving a vertical selection signal in response to a vertical shift clock signal and generating an internal vertical selection signal to enable a first horizontal line or a second horizontal line among the m horizontal lines;

a vertical erasure signal generator for receiving a system clock signal, generating a vertical erasure signal for erasing a charge signal of a horizontal line, and applying the vertical erasure signal to the first or second horizontal line; and

a vertical transmission signal generator for receiving the system clock signal, generating a vertical transmission signal for outputting a charge signal of a horizontal

line, and applying the vertical transmission signal to the first horizontal line and a horizontal line following the first horizontal line.

17. The high-speed image pickup controller of claim 16, wherein the first horizontal line is an arbitrary horizontal line among the m horizontal lines.

18. The high-speed image pickup controller of claim 16, wherein the second horizontal line is an arbitrary horizontal line between the first horizontal line and the m-th horizontal line.

19. The high-speed image pickup controller of claim 16, wherein the vertical erasure signal is enabled twice during a single period of a horizontal synchronizing signal.

20. The high-speed image pickup controller of claim 16, wherein a rate at which the vertical shift clock signal is enabled can be adjusted.